

CLAIMS

What is claimed is:

- 1 1. A capacitor comprising:
 - 2 m electrode plates;
 - 3 wherein each of said m electrode plates are arranged spaced apart in parallel;
 - 4 wherein m is an integer greater than 1;
 - 5 wherein each of said m electrode plates comprises a first extension;
 - 6 n first external terminals;
 - 7 wherein n is an integer greater than 1;
 - 8 wherein said n first external terminals are arranged on a first common exterior surface of the capacitor;
 - 9 wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals;
 - 10 wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals;
 - 11 wherein said n first external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance.

- 1 2. The capacitor of claim 1, wherein said predefined minimal distance is a minimal distance that prevents crosstalk between said n first external terminals.

- 1 3. The capacitor of claim 1, wherein said n first external terminals are arranged in parallel.

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1 4. The capacitor of claim 1, wherein n=2; wherein said n first external terminals are
2 arranged in parallel.

1 5. The capacitor of claim 1, wherein n=3; wherein said n first external terminals are
2 arranged in parallel and wherein said even one of said n first external terminals is arranged
3 between the odd ones of said n first external terminals.

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1 6. The capacitor of claim 1, wherein a dielectric material is disposed between each of
2 said m electrode plates.

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1 7. The capacitor of claim 6, wherein said dielectric material is ceramic material.

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1 8. The capacitor of claim 1, wherein exterior ones of said n first external terminals are
2 disposed on said common exterior surface of said capacitor and corresponding side surfaces
3 of said capacitor.

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1 9. The capacitor of Claim 1, wherein n is 4;

2 wherein a first one and a second one of said n first external terminals are
3 arranged in a first row;

4 wherein a third one and a fourth one of said n first external terminals are
5 arranged in a second row;

6 wherein said first one of said n first external terminals is arranged adjacent said
7 second and fourth ones of said n first external terminals and diagonal to said third one
8 of said n first external terminals;

9 wherein said second one of said n first external terminals is arranged diagonal to said
10 fourth one of said n first external terminals.

1 10. The capacitor of Claim 1,
2 wherein each of said m electrode plates comprises a second extension;
3 wherein said capacitor comprises s second external terminals;
4 wherein s is an integer greater than 1;
5 wherein said s second external terminals are arranged on a second common
6 exterior surface of the capacitor;
7 wherein said second extensions of said even ones of said m electrode plates are
8 coupled to said even ones of said s second external terminals;
9 wherein said second extensions of said odd ones of said m electrode plates are
10 coupled to odd ones of said s second external terminals.

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1 11. The capacitor of Claim 10, wherein said second common exterior surface is
2 arranged opposite to said first common exterior surface.

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1 12. The capacitor of Claim 1,
2 wherein each of said m electrodes comprises a second extension;
3 wherein the capacitor comprises s second external terminals;
4 wherein s is an integer greater than 1;
5 wherein even ones of said s second external terminals are arranged on a third
6 exterior surface of the capacitor;
7 wherein odd ones of said s second external terminals are arranged on a fourth
8 exterior surface of the capacitor;
9 wherein said second extensions of even ones of said m electrode plates are
10 coupled to even ones of said s second external terminals; and
11 wherein said second extensions of odd ones of said m electrode plates are coupled
12 to odd ones of said s second external terminals.

1 13. The capacitor of Claim 12, wherein said third exterior surface is arranged opposite
2 to said fourth exterior surface.

1 14. The capacitor of claim 1, further comprising a housing that encloses at least a part
2 of said capacitor.

1 15. The capacitor of claim 1, wherein height of said capacitor is greater than width of
2 said capacitor.

1 16. The capacitor of claim 1, wherein a portion of at least one of said n first external
2 terminals wraps around a corner of said capacitor.

1 17. The capacitor of claim 1, wherein said n first external terminals have a bar
2 structure.

1 18. A filter comprising:

2 an inductor;

3 a capacitor of Claim 1,

4 wherein said inductor is connected to even ones of said n first external terminals;

5 wherein an output terminal is connected to even ones of said n first external
6 terminals; and

7 wherein a reference voltage is connected to odd ones of said n first external
8 terminals.

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1 19. The filter of claim 18,
2 wherein n=3;
3 wherein said n first external terminals are arranged in parallel and wherein said even
4 one of said n first external terminals is arranged between the odd ones of said n
5 first external terminals;
6 wherein first and third ones of said n first external terminals are coupled to
7 the reference voltage;
8 wherein one terminal of said inductor is coupled to a first end portion of a
9 second one of said n first external terminals; and
10 wherein the output terminal of said filter is provided at a second end
11 portion of said second one of said n first external terminals.

1 20. The filter of claim 18,
2 wherein n=2;
3 wherein said n first external terminals are arranged in parallel;
4 wherein first one of said n first external terminals is coupled to a reference
5 voltage ;
6 wherein one terminal of said inductor is coupled to a first end portion of a
7 second one of said n first external terminals; and
8 wherein an output terminal of said filter is provided at a second end
9 portion of said second one of said n first external terminals.

1 21. A voltage regulator comprising the filter of claim 18.
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1 22. The voltage regulator of claim 21 further comprising a multilayer printed circuit
2 board;
3 wherein said capacitor is mounted on said multilayer printed circuit board;
4 wherein said inductor is connected to a first trace of said multilayer printed circuit
5 board;
6 wherein said first trace is connected to said even ones of said n first external terminals
7 by way of a first plurality of vias;
8 wherein said output terminal is connected to a second trace on said multilayer printed
9 circuit board;
10 wherein said second trace is connected to said even ones of said n first external
11 terminals by way of a second plurality of vias;
12 wherein the reference voltage is connected to a third trace on said multilayer printed
13 circuit board; and
14 wherein said third trace is connected to said odd ones of said n first external terminals
15 by way of a third plurality of vias.

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1 23. A printed circuit board (“PCB”) comprising:
2 a plurality of PCB contacts; and
3 a plurality of capacitors of Claim 1 coupled to said plurality of PCB contacts to
4 facilitate parallel connections of at least two capacitors.

1 24. A capacitor structure comprising:
2 a first capacitor comprising:
3 m electrode plates;
4 wherein each of said m electrode plates are arranged spaced apart in parallel;

5 wherein m is an integer greater than 1;
6 wherein each of said m electrodes comprises a first extension;
7 wherein each of said m electrodes comprises a second extension;
8 n first external terminals;
9 wherein n is an integer greater than 1;
10 wherein said n first external terminals are arranged on a first common
11 exterior surface of said first capacitor;
12 wherein said first extension of even ones of said m electrode plates are
13 coupled to even ones of said n first external terminals;
14 wherein said first extension of odd ones of said m electrode plates are
15 coupled to odd ones of said n first external terminals;
16 s second external terminals;
17 wherein s is an integer greater than 1;
18 wherein said s second external terminals are arranged on a second common
19 exterior surface of the first capacitor;
20 wherein said second extension of even ones of said m electrode plates are
21 coupled to even ones of said s second external terminals;
22 wherein said second extension of odd ones of said m electrode plates are coupled to
23 odd ones of said s second external terminals
24 a second capacitor comprising:
25 x electrode plates;
26 wherein each of said x electrode plates are arranged in parallel;
27 wherein x is an integer greater than 1;
28 wherein each of said x electrodes comprises a third extension;
29 s third external terminals;

30 wherein said s third external terminals are arranged on a third common
31 exterior surface of said second capacitor;
32 wherein said third extension of even ones of said x electrode plates are
33 coupled to even ones of said s third external terminals;
34 wherein said third extension of odd ones of said x electrode plates are
35 coupled to odd ones of said s third external terminals;
36 wherein said second capacitor is mounted on said first capacitor; and
37 wherein said s third external terminals are coupled to corresponding ones of
38 said s second external terminals.

1 25. The capacitor structure of claim 24, further comprising a housing that encloses at
2 least a part of said first and said second capacitors.

1 26. The capacitor structure of claim 24, wherein said n first external terminals are
2 arranged in parallel; wherein said s second external terminals are arranged in parallel; and
3 wherein said s third external terminals are arranged in parallel.

1 27. The capacitor structure of claim 24, wherein s=2; wherein said s second external
2 terminals are arranged in parallel and wherein said s third external terminals are arranged in
3 parallel.

1 28. The capacitor structure of claim 24, wherein s=3; wherein said s second external
2 terminals are arranged in parallel and wherein said even one of said s second external
3 terminals is arranged between the odd ones of said s second external terminals and wherein
4 said s third external terminals are arranged in parallel and wherein said even one of said s
5 third external terminals is arranged between the odd ones of said s third external terminals.

1 29. The capacitor structure of claim 24, wherein a first dielectric material is disposed
2 between each of said m electrode plates of said first capacitor; and wherein a second dielectric
3 material is disposed between each of said x electrode plates of said second capacitor.

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1 30. The capacitor structure of 29, wherein said first and second dielectric material are
2 different.

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1 31. The capacitor structure of 29, wherein said first and second dielectric material are
2 the same.

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1 32. The capacitor structure of claim 29, wherein at least one of said first dielectric
2 material and said second dielectric material comprises a ceramic material.

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1 33. The capacitor structure of Claim 24, wherein s is 4;
2 wherein a first one and a second one of said s second external terminals are arranged
3 in a first row;

4 wherein a third one and a fourth one of said s second external terminals are arranged
5 in a second row;

6 wherein said first one of said s second external terminals is arranged adjacent to said
7 second and fourth ones of said s second external terminals and diagonal to said
8 third one of said s second external terminals;

9 wherein said second one of said s second external terminals is arranged diagonal to
10 said fourth one of said s second external terminals;

11 wherein a first one and a second one of said s third external terminals are arranged in a
12 first row;

13 wherein a third one and a fourth one of said s third external terminals are arranged in a
14 second row;
15 wherein said first one of said s third external terminals is arranged adjacent to said
16 second and fourth ones of said s third external terminals and diagonal to said
17 third one of said s third external terminals; and
18 wherein said second one of said s third external terminals is arranged diagonal to said
19 fourth one of said s third external terminals.

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1 34. The capacitor structure of Claim 24,
2 wherein each of said x electrodes plates comprises a fourth extension;
3 wherein said capacitor comprises u fourth external terminals;
4 wherein u is an integer greater than 1;
5 wherein said u fourth external terminals are arranged on a fourth common exterior
6 surface of said second capacitor;
7 wherein said fourth extensions of said even ones of said x electrode plates are coupled
8 to said even ones of said u fourth external terminals;
9 wherein said fourth extensions of said odd ones of said x electrode plates are coupled
10 to odd ones of said u fourth external terminals.

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1 35. The capacitor structure of Claim 34, wherein said third common exterior surface
2 is arranged opposite to said fourth common exterior surface.

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1 36. The capacitor structure of claim 24, wherein said s second and s third external
2 terminals have a bar structure.

1 37. A filter comprising:
2 an inductor;
3 a capacitor structure of Claim 24;
4 wherein said inductor is connected to even ones of said n first external terminals;
5 wherein an output terminal is connected to even ones of said n first external terminals;
6 and
7 wherein a reference voltage is connected to odd ones of said n first external terminals.

1 38. The filter of claim 37, wherein n=3;
2 wherein said n first external terminals are arranged in parallel and wherein said even
3 one of said n first external terminals is arranged between the odd ones of said n
4 first external terminals;
5 wherein first and third ones of said n first external terminals are coupled to the
6 reference voltage;
7 wherein one terminal of said inductor is coupled to a first end portion of a second one
8 of said n first external terminals; and
9 wherein the output terminal of said filter is provided at a second end portion of said
10 second one of said n first external terminals.

1 39. The filter of claim 37, wherein n=2;
2 wherein said n first external terminals are arranged in parallel;
3 wherein first one of said n first external terminals is coupled to a reference voltage;
4 wherein one terminal of said inductor is coupled to a first end portion of a second one
5 of said n first external terminals; and
6 wherein an output terminal of said filter is provided at a second end portion of said
7 second one of said n first external terminals.

1 40. A voltage regulator comprising the filter of claim 37 further comprising a
2 multilayer printed circuit board; wherein said capacitor structure is mounted on
3 said multilayer printed circuit board;
4 wherein said inductor is connected to a first trace of said multilayer printed circuit
5 board; and
6 wherein said first trace is connected to said even ones of said n first external terminals
7 by way of a first plurality of vias;
8 wherein said output terminal is connected to a second trace on said multilayer printed
9 circuit board;
10 wherein said second trace is connected to said even ones of said n first external
11 terminals by way of a second plurality of vias;
12 wherein the reference voltage is connected to a third trace on said multilayer printed
13 circuit board; and
14 wherein said third trace is connected to said odd ones of said n first external terminals
15 by way of a third plurality of vias.

1 41. A capacitor structure comprising:
2 a first capacitor comprising:
3 m electrode plates;
4 wherein each of said m electrode plates are arranged spaced apart in
5 parallel;
6 wherein m is an integer greater than 1;
7 wherein each of said m electrodes comprises a first extension and a second
8 extension;
9 n first external terminals;

10 wherein n is an integer greater than 1;
11 wherein said n first external terminals are arranged on a first common
12 exterior surface of said first capacitor;
13 wherein said first extension of even ones of said m electrode plates are
14 coupled to even ones of said n first external terminals;
15 wherein said first extension of odd ones of said m electrode plates are
16 coupled to odd ones of said n first external terminals;;
17 s second external terminals;
18 wherein s is an integer greater than 0;
19 wherein said s second external terminals are arranged on a second common
20 exterior surface of the first capacitor;
21 wherein said second extension of even ones of said m electrode plates are
22 coupled to said s second external terminals;
23 a second capacitor comprising:
24 x electrode plates;
25 wherein each of said x electrode plates are arranged spaced apart in
26 parallel;
27 wherein x is an integer greater than 1;
28 wherein each of said x electrodes comprises a third extension;
29 s third external terminals;
30 wherein said s third external terminals are arranged on a third common
31 exterior surface of said second capacitor;
32 wherein said third extension of even ones of said x electrode plates are
33 coupled to said s third external terminals;
34 wherein said second capacitor is disposed adjacent to said first capacitor;

35 wherein said s third external terminals are coupled to corresponding ones of
36 said s second terminals.

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1 42. The capacitor structure of claim 41, wherein said n first external terminals are
2 arranged in parallel; wherein said s second external terminals are arranged in parallel; and
3 wherein said s third external terminals are arranged in parallel.

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1 43. The capacitor structure of claim 41, wherein s=2; wherein said s second external
2 terminals are arranged in parallel and wherein said s third external terminals are arranged in
3 parallel.

1 44. The capacitor structure of claim 41, wherein s=3; wherein said s second external
2 terminals are arranged in parallel and wherein said even one of said s second external
3 terminals is arranged between the odd ones of said n second external terminals and wherein
4 said s third external terminals are arranged in parallel and wherein said even one of said s
5 third external terminals is arranged between the odd ones of said s third external terminals.

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1 45. The capacitor structure of claim 41, wherein a first dielectric material is disposed
2 between each of said m electrode plates of said first capacitor; and wherein a second dielectric
3 material is disposed between each of said x electrode plates of said second capacitor.

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1 46. The capacitor structure of 45, wherein said first and second dielectric material are
2 different.

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1 47. The capacitor structure of 45, wherein said first and second dielectric material are
2 the same.

1 48. The capacitor of claim 41, wherein said n first external terminals are arranged in
2 parallel.

1 49. The capacitor of claim 41, wherein n=2; wherein said n first external terminals are
2 arranged in parallel.

1 50. The capacitor of claim 41, wherein n=3; wherein said n first external terminals are
2 arranged in parallel and wherein said even one of said n first external terminals is arranged
3 between the odd ones of said n first external terminals.

1 51. The capacitor of claim 45, wherein at least one of said first second dielectric
2 material and said second dielectric material comprises a ceramic material.

1 52. The capacitor of Claim 41, wherein n is 4;
2 wherein a first one and a second one of said n first external terminals are arranged in a
3 first row;
4 wherein a third one and a fourth one of said n first external terminals are arranged in a
5 second row;
6 wherein said first one of said n first external terminals is arranged adjacent to said
7 second and fourth ones of said n first external terminals and diagonal to said
8 third one of said n first external terminals; and
9 wherein said second one of said n first external terminals is arranged diagonal to said
10 fourth one of said n first external terminals.

1 53. The capacitor of claim 41, wherein said n first external terminals have a bar
2 structure.

1 54. A filter comprising:
2 an inductor;
3 a capacitor of Claim 41;
4 wherein said inductor is connected to even ones of said n first external terminals;
5 wherein an output terminal is connected to even ones of said n first external terminals;
6 and
7 wherein a reference voltage is connected to odd ones of said n first external terminals.

1 55. The filter of claim 54, wherein n=3;
2 wherein said n first external terminals are arranged in parallel and wherein said even
3 one of said n first external terminals is arranged between the odd ones of said n
4 first external terminals;
5 wherein first and third ones of said n first external terminals are coupled to the
6 reference voltage;
7 wherein one terminal of said inductor is coupled to a first end portion of a second one
8 of said n first external terminals; and
9 wherein the output terminal of said filter is provided at a second end portion of said
10 second one of said n first external terminals.

1 56. The filter of claim 54, wherein n=2;
2 wherein said n first external terminals are arranged in parallel;
3 wherein first one of said n first external terminals is coupled to a reference voltage;
4 wherein one terminal of said inductor is coupled to a first end portion of a second one
5 of said n first external terminals; and
6 wherein an output terminal of said filter is provided at a second end portion of said
7 second one of said n first external terminals.

1 57. A voltage regulator comprising the filter of claim 54 further comprising a
2 multilayer printed circuit board; wherein said capacitor structure is mounted on
3 said multilayer printed circuit board;
4 wherein said inductor is connected to a first trace of said multilayer printed circuit
5 board; and
6 wherein said first trace is connected to said even ones of said n first external terminals
7 by way of a first plurality of vias;
8 wherein said output terminal is connected to a second trace on said multilayer printed
9 circuit board;
10 wherein said second trace is connected to said even ones of said n first external
11 terminals by way of a second plurality of vias;
12 wherein the reference voltage is connected to a third trace on said multilayer printed
13 circuit board; and
14 wherein said third trace is connected to said odd ones of said n first external terminals
15 by way of a third plurality of vias.

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1 58. The filter of claim 54, wherein s=1;
2 wherein said s second external terminal is coupled to even ones of said m electrode
3 plates; and
4 wherein said s third external terminal is coupled to even ones of said x electrode
5 plates.

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1 59. The capacitor structure of claim 41, wherein at least one of said s second external
2 terminals extend from said second common exterior surface to said first
3 common exterior surface of said first capacitor by wrapping around a corner of
4 said first capacitor.

1 60. A printed circuit board ("PCB") comprising:
2 a plurality of PCB contacts; and
3 a plurality of capacitor structures of Claim 41 coupled to said plurality of PCB
4 contacts to provide parallel connections of at least two capacitors.

1 61. A device comprising:
2 a first capacitor comprising;
3 m electrode plates;
4 wherein each of said m electrode plates are arranged spaced apart in
5 parallel;
6 wherein m is an integer greater than 1;
7 wherein each of said m electrodes comprises a first extension;
8 wherein w electrode plates of said m electrode plates comprise a second
9 extension, wherein w is an integer less than m;
10 n first external terminals;
11 wherein n is an integer greater than 1;
12 wherein said n first external terminals are arranged on a first common
13 exterior surface of said first capacitor;
14 wherein said first extension of even ones of said m electrode plates are
15 coupled to even ones of said n first external terminals;
16 wherein said first extension of odd ones of said m electrode plates are
17 coupled to odd ones of said n first external terminals;
18 s second external terminals;
19 wherein s is an integer greater than 1;

20 wherein said s second external terminals are arranged on a second common
21 exterior surface of the first capacitor;
22 wherein said second extension of even ones of said w electrode plates are
23 coupled to even ones of said s second external terminals;
24 wherein said second extension of odd ones of said w electrode plates are
25 coupled to odd ones of said s second external terminals;
26 a second capacitor comprising:
27 x electrode plates;
28 wherein each of said x electrode plates are arranged spaced apart in
29 parallel;
30 wherein x is an integer greater than 1;
31 wherein y electrode plates of said x electrode plates comprise a third extension;
32 wherein y is an integer less than x;
33 q third external terminals;
34 wherein q is an integer greater than 1;
35 wherein said q third external terminals are arranged on a third common
36 exterior surface of said second capacitor;
37 wherein said third extension of even ones of said y electrode plates are
38 coupled to even ones of said q third external terminals;
39 wherein said third extension of odd ones of said y electrode plates are
40 coupled to odd ones of said q third external terminals;
41 wherein said second capacitor is disposed abutting and adjacent to said first
42 capacitor;
43 wherein said even ones of said q third external terminals are coupled to said
44 even ones of said s second terminals; and

45 wherein said odd ones of said q third external terminals are coupled to said odd
46 ones of said s second terminals.

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1 62. The device of claim 61,

2 wherein z electrode plates of said m electrode plates comprise a fourth extension ;

3 wherein sum of y and z is integer less than or equal to m;

4 wherein the first capacitor further comprises f fourth external terminals;

5 wherein f is an integer greater than 1;

6 wherein said f fourth external terminals are arranged on a fourth common

7 exterior surface of said first capacitor; wherein said fourth common

8 exterior surface is opposite to said second common exterior surface;

9 wherein said fourth extension of even ones of said z electrode plates are

10 coupled to even ones of said f fourth external terminals; and

11 wherein said third extension of odd ones of said z electrode plates are

12 coupled to odd ones of said f fourth external terminals.

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1 63. A circuit comprising:

2 a printed circuit board (“PCB”) including a plurality of PCB contacts longitudinally
3 arranged in parallel; and

4 a plurality of capacitors wherein each of said capacitors is arranged abutting with each
5 other and mounted on said PCB; wherein each of said plurality of capacitors
6 comprises said capacitor of Claim 1.

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1 64. The capacitor of Claim 10, wherein said second common exterior surface is
2 arranged substantially orthogonal to said first common exterior surface. .

1 65. The capacitor of Claim 12, wherein said third and fourth common exterior
2 surfaces are arranged substantially orthogonal to said first common exterior
3 surface. .

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1 66. The capacitor of Claim 1,
2 wherein each of said m electrodes comprises a second extension;
3 wherein the capacitor comprises s second external terminals;
4 wherein s is an integer greater than 1;
5 wherein even ones of said s second external terminals are arranged on a third
6 exterior surface of the capacitor;
7 wherein odd ones of said s second external terminals are arranged on a third
8 exterior surface of the capacitor;
9 wherein said second extensions of even ones of said m electrode plates are
10 coupled to even ones of said s second external terminals; and
11 wherein said second extensions of odd ones of said m electrode plates are coupled
12 to odd ones of said s second external terminals.

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1 66. The capacitor of Claim 66, wherein said odd ones of said s second external
2 terminals are arranged space apart and parallel to said even ones of said s
3 second external terminals. .

1 67. The capacitor of claim 14, wherein said housing is formed from an ejection
2 molding process.

1 68. The capacitor of claim 1, further comprising an encapsulation that encloses at
2 least a part of said capacitor.

1 69. The capacitor of Claim 24, wherein said second common exterior surface is
2 arranged substantially orthogonal to said first common exterior surface. .

1 70. The capacitor structure of claim 25, wherein said housing is formed from an
2 ejection molding process.

1 71. The capacitor structure of claim 24, further comprising an encapsulation that
2 encloses at least a part of said first and second capacitors.

1 72. The capacitor structure of Claim 24,
2 wherein each of said x electrodes plates comprises a fourth extension;
3 wherein said capacitor comprises u fourth external terminals;
4 wherein u is an integer greater than 1;
5 wherein said u fourth external terminals are arranged on said third common exterior
6 surface of said second capacitor;
7 wherein said fourth extensions of said even ones of said x electrode plates are coupled
8 to said even ones of said u fourth external terminals;
9 wherein said fourth extensions of said odd ones of said x electrode plates are coupled
10 to odd ones of said u fourth external terminals.

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1 73. The capacitor structure of Claim 41, wherein said second common exterior
2 surface is arranged substantially orthogonal to said first common exterior surface,
3 wherein said third common exterior surface is arranged substantially orthogonal to
4 said fourth common exterior surface. .

1 74. The device of claim 61, further comprising a housing that encloses at least a part
2 of said device. .

1 75. The device of claim 74, wherein said housing is formed from an ejection molding
2 process.

1 76. The device of claim 61, further comprising an encapsulation that encloses at least
2 a part of said device.

1 77. The device of claim 1, wherein the predefined minimal distance is less than 12
2 mils.

1 78. The device of claim 1, wherein the predefined minimal distance is less than 8
2 mils.

1 79. The capacitor structure of claim 25, wherein the housing comprises a fin to
2 dissipate heat from said first and second capacitors..